UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,082	01/07/2002	Christopher Michael Abernathy	AUS920010807US1	6560

7590	11/23/2004	

Gregory W. Carr
Carr & Storm, L.L.P.
670 Founders Square
900 Jackson Street
Dallas, TX 75202

EXAMINER
CHEN, TSE W

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>07 January 2002</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-16</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-16</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>07 January 2002</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)	4)☐ Interview Summary (PTO-413)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)	5)☐ Notice of Informal Patent Application (PTO-152)
Paper No(s)/Mail Date _____ .	6)☐ Other: _____ .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Re Claims 1-3, 8, 11-13

2.   Claims 1-3, 8, 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Fletcher

et al., US Patent 6611920, hereinafter Fletcher.

3.   In re claim 1, Fletcher discloses a microprocessor [integrated circuit] configured for

executing at least one instruction, the microprocessor having a main processor clock [fig.3;

abstract], the microprocessor comprising:

- A first stage [310.1] having one or more storage components [inherently, a storage

   component in the broadest interpretation is needed to receive data for processing]

   configured for storing operand data of the at least one instruction, the first stage being

   clocked by at least a first clock [320.1] derived from the main processor clock [col.4, ll.6-

   26].

- A first combinatorial logic [310.1] connected to the first stage for receiving the operand

   data from the first stage and configured for processing the operand data and generating

   first output data, wherein the first clock is operational only during a first period of time

   when the operand data is processed by the first combinatorial logic [col.4, ll.1-60].

- A second stage [310.2] of one or more storage components [inherently, a storage component in the broadest interpretation is needed to receive data for processing] configured for storing the first output data, the second stage being clocked by at least a second clock derived from the main processor clock [col.4, ll.6-26].

- A second combinatorial logic [310.2] connected to the second stage for receiving the first output data from the second stage and configured for processing the first output data and generating second output data, wherein the second clock is operational only during a second period of time when the first output data is processed by the second combinatorial logic [col.4, ll.1-60].

4.   As to claim 2, Fletcher discloses the microprocessor comprising:

- A first local clock buffer [320.1] connected to the first stage for providing at least the first clock to the first stage only during the first period of time [col.4, ll.1-60].

- A second local clock buffer [320.2] configured for generating the second clock and connected to the second stage for providing at least the second clock to the second stage only during the second period of time [col.4, ll.1-60].

5.   As to claim 3, Fletcher discloses each and every limitation of the claim as discussed above in reference to claim 2, including:

- A dynamic clock-control unit [330.1 and 340.1] connected to at least the first local clock buffer for providing a first control signal [output of 330.1] to at least the first local clock buffer and configured for generating the first control signal, the first control signal enabling the first clock signal to be operational only during the first period of time [col.4, ll.15-60].

6.   As to claim 8, Fletcher discloses the microprocessor wherein the second period of time is

automatically determined by delaying the first period of time by one cycle of the main processor

clock [col.4, ll.27-57].

7.   In re claim 11, Fletcher discloses each and every limitation of the claim as discussed

above in reference to claims 1 and 3. Fletcher discloses the microprocessor; therefore, Fletcher

discloses the method of using the microprocessor.

8.   As to claim 12, Fletcher discloses each and every limitation of the claim as discussed

above in reference to claims 11 and 2.

9.   As to claim 13, Fletcher discloses each and every limitation of the claim as discussed

above in reference to claims 11 and 3.

Claim Rejections - 35 USC § 103

10.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

Re Claims 4-7, 9, 14-16

11.   Claims 4-7, 9, 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Fletcher as applied to claim 1 above, and further in view of Sutherland, US Patent 6304125.

12.   In re claim 4, Fletcher discloses each and every limitation of the claim as discussed above

in reference to claim 1. Fletcher did not discuss the details of data origination or destination.

13.   Sutherland discloses a microprocessor [abstract], comprising an integrated storage

component [12] configured for storing the operand data, the integrated storage component being

connected to the first stage [s1] for providing the operand data to the first stage and being

connected to the second combinatorial logic [s5] for receiving the second output data from the

second combinatorial logic [fig.1; col.3, l.55 – col.4, l.17].

14.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Fletcher and Sutherland before him at the time the invention was made, to modify the

microprocessor taught by Fletcher to include the integrated storage component taught by

Sutherland, as the integrated storage component taught by Sutherland is a well known

component suitable for use with the microprocessor of Fletcher. One of ordinary skill in the art

would have been motivated to make such a combination as it provides a way to store operands

before and after pipeline processing [Sutherland: col.3, l.55 – col.4, l.17].

15.   As to claim 5, Fletcher and Sutherland disclose each and every limitation of the claim as

discussed above in reference to claims 2 and 4.

16.   As to claim 6, Sutherland discloses the microprocessor wherein the first stage comprises

one or more latches, and wherein the second stage comprises one or more latches [col.3, l.55 –

col.4, l.17].

17.   As to claim 7, Sutherland discloses a microprocessor [abstract], comprising an integrated

storage component [12] configured for storing the operand data, the integrated storage

component being connected to the first stage [s1] for providing the operand data to the first stage

and being connected to the second combinatorial logic [s5] for receiving the second output data

from the second combinatorial logic, wherein the integrated storage component comprises an

array [register file] [fig.1; col.3, l.55 – col.4, l.17].

18.   As to claim 9, Fletcher and Sutherland disclose each and every limitation of the claim as discussed above in reference to claims 3 and 4.

19.   As to claim 14, Fletcher discloses each and every limitation of the claim as discussed above in reference to claims 11 and 4.

20.   As to claim 15, Fletcher discloses each and every limitation of the claim as discussed above in reference to claims 11 and 5.

21.   As to claim 16, Fletcher discloses each and every limitation of the claim as discussed above in reference to claims 11 and 9.

Re Claim 10

22.   Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fletcher as applied to claim 1 above, and further in view of Kopser et al., US Patent 6629250, hereinafter Kopser.

23.   Fletcher taught each and every limitation of the claim, as discussed above in reference to claim 1. Fletcher did not discuss the details of the stage components.

24.   Kopser discloses a storage component comprising a master latch [20] configured for storing an operand data and being clocked by a first master clock [ckm] derived from a first clock [ck] and a slave latch [22] connected to the master latch for receiving the operand data [dm] from the master latch and storing the operand data, the slave latch being configured for being clocked by a first slave clock [36] derived from the first clock [fig.2; col.3, l.31 – col.4, l.4].

25.   It would have been obvious to one of ordinary skill in the art, having the teachings of Fletcher and Kopser before him at the time the invention was made, to modify the

microprocessor taught by Fletcher to include the storage component taught by Kopser, in order to obtain the microprocessor wherein each storage component in the first stage comprises a master latch configured for storing the operand data and being clocked by a first master clock derived from the first clock and a slave latch connected to the master latch for receiving the operand data from the master latch and storing the operand data, the slave latch being configured for being clocked by a first slave clock derived from the first clock. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to ensure synchronization of data transfer [Kopser: col.1, 1.14 – col.2, 1.43].

Conclusion

26.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additionally cited U.S. patent documents describe various systems and methods related to pipeline processing and clock control.
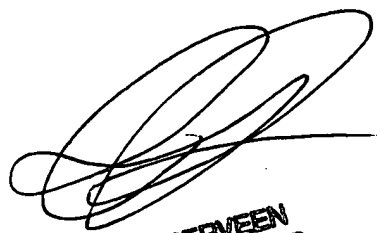
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
November 18, 2004

REHANA PERVEEN
PRIMARY EXAMINER